REMARKS

Applicants respectfully request the Examiner's consideration of the present application as amended. Claims 1 and 14-20 remain in the application. New claims 21-32 have been added. Claims 1, 15, 16 and 18 have been amended. Therefore, claims 1 and 14-32 are currently pending.

The Examiner objected to claim 16. Claim 16 has been amended, in accordance with Examiner's suggestion.

The Examiner objected to the drawings, as filing to show every feature of the invention specified in the claims. The Examiner stated that the step of "determining if the system bus is controlled for configuration by a first device" was not shown in the Figures. Examiner further objected to the Specification as failing to provide antecedent basis for the claimed subject matter. Examiner rejected claims 1 and 14-20 under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors at the time the application was filed, had possession of the claimed invention.

Applicants have amended claim 1 to remove the language objected to, which was the basis for the rejections. The current language "controlling the system bus for configuration using a first device" finds support in the Figures and the Specification, for example in Figure 2, where the system bus 205 is seen as controlled by either the CPU 206, or DMA controller 207. Furthermore, in Figure 3A, block 320 reads "configure CSL." In the corresponding discussion in the specification, at page 12, lines 1-3 and lines 16-28, it is clarified that one of a plurality of devices may control the multi-master

system bus for configuration. Therefore, applicants submit that the amended claims are supported by the current figures and specification.

Applicants further submit that the amended and the new claims are not anticipated by or rendered obvious over U.S. Pat. No. 5,361,373 of Gilson ("Gilson") and U.S. Pat. No. 5,668,815 of Gittinger et al. ("Gittinger"), alone or in combination.

Gilson discloses an integrated circuit computing device wherein:

> Host 40 reconfigures the FPGA 12 which causes new configuration data to be written into the Configuration Memory Array 20. Now referring to FIG. 2, the effect of this new configuration data is to . . . change the programming of the Logic Blocks 34 that comprise the Reconfigurable Instruction Execution Unit 16 such that the desired complex operation can be accomplished by the newly configured hardware on data that already exists within the Reconfigurable Instruction Execution Unit 16.

(Gilson Col. 7, lines 22-35).

Gilson discloses that host 40 reconfigures the FPGA 12 (col. 7 line 22). Gilson fails to teach or suggest controlling the system bus for configuration using a first device, selected from among a group. Rather, Gilson discusses only a single possible device, Host 40, that may configure the FPGA. Additionally, Gilson fails to disclose that FPGA 12 has a DMA controller with which to control the system bus for configuration.

Claim 1, as amended, on the other hand, recites:

> A method of using a system bus on a configurable system on a chip (CSoC), the CSoC including configurable system logic (CSL), the method comprising:
> controlling the system bus for configuration using a first device, the first device comprising a selectable one of an on-chip central processing unit (CPU), a direct memory access (DMA) controller, and an external control device;
> configuring a memory cell in the CSL using the system bus; and
> reading the memory cell in the CSL using the system bus.

(Claim 1, as amended). As noted above, Gilson does not teach or suggest controlling a system bus for configuration using a first device, selected from among a

group. Furthermore, Gilson does not teach or suggest a DMA controller controlling a system bus for configuration. Therefore, claim 1, as amended, is not anticipated by or obvious over Gilson. Claims 2-3 and 14-20 depend on claim 1, and incorporate its limitations. Therefore, for at least the same reasons advanced above with respect to claim 1, claims 14-20 are not anticipated by or obvious over Gilson.

New claim 21 recites:

> A method of configuring a configurable system on a chip (CsoC) comprising:
> initiating configuration of the CsoC using an on-chip central processing unit (CPU);
> passing control of a system bus to a first device for configuring on-chip configurable system logic (CSL);
> configuring a memory cell in the CSL using the first device.

(Claim 21). Gilson does not teach or suggest passing control of a system bus to a first device for configuring a CSL. Rather, Gilson states that Host 40 reconfigures the FPGA. Therefore, claim 21, and claims 22-29 which depend on it, are not anticipated by or obvious over Gilson.

Claim 30 recites:

> A method comprising:
> initiating configuration of a configurable system on chip (CsoC) using an on-chip central processing unit (CPU);
> configuring a memory cell in the CSL using a first device of a group of devices, the group of devices comprising the CPU, a direct memory access (DMA) controller, and an external control device;
> reading a memory cell in the CSL using a second device selected from the group of devices; and
> selecting a signal in the CSoC to determine if the system bus is used for configuration or general interconnect of the CSoC.

(Claim 30). As noted above, Gilson does not teach or suggest configuring a memory cell using a device selected from a group of devices. Furthermore, Gilson does not teach or suggest reading a memory cell using a second device selected from

the group of devices. Therefore, claim 30, and claims 31 and 32 which depend on it, are not anticipated by or obvious over Gilson.

Gittinger states that a

> Microcontroller 10 includes a clock/power management unit 12, an interrupt control unit 14, a processor core 16, a timer control unit 18, a DMA control unit 20, a programmable input/output (PIO) unit 22, an asynchronous serial interface 24, a synchronous serial interface 26, a chip select unit 28, an internal memory 30, and a bus interface unit 32.

(Gittinger Col. 5, lines 19-26). The microcontroller of Gittinger does not include configurable a configurable system logic ("CSL"). Applicants respectfully submit that the internal memory 30 of Gittinger is not a configurable system logic. Internal memory is generally random access memory (RAM) or similar memory. This is distinct from configurable system logic, as claimed in the present invention.

Claim 1, as amended, on the other hand, recites:

> A method of using a system bus on a configurable system on a chip (CSoC), the CSoC including configurable system logic (CSL), the method comprising:
> controlling the system bus for configuration using a first device, the first device comprising a selectable one of an on-chip central processing unit (CPU), a direct memory access (DMA) controller, and an external control device;
> configuring a memory cell in the CSL using the system bus; and
> reading the memory cell in the CSL using the system bus.

(Claim 1, as amended). As noted above, Gittinger does not teach or suggest controlling a system bus for configuration of a CSL using a first device, selected from among a group. Furthermore, Gittinger does not teach or suggest configuring a memory cell in a configurable system logic. Therefore, claim 1, as amended, is not anticipated by or obvious over Gittinger. Claims 2-3 and 14-20 depend on claim 1, and incorporate its limitations. Therefore, for at least the same reasons advanced above with respect to claim 1, claims 14-20 are not anticipated by or obvious over Gittinger.

New claim 21 recites:

> A method of configuring a configurable system on a chip (CsoC) comprising:
> initiating configuration of the CsoC using an on-chip central processing unit (CPU);
> passing control of a system bus to a first device for configuring on-chip configurable system logic (CSL);

configuring a memory cell in the CSL using the first device. (Claim 21). Gittinger does not teach or suggest passing control of a system bus to a first device for configuring a CSL. Rather, Gittinger states that a DMA may be used to test memory. However, a memory test of a RAM or similar internal memory is dissimilar from configuring a memory cell in a configurable system logic, as recited in claim 21. Therefore, claim 21, and claims 22-29 which depend on it, are not anticipated by or obvious over Gittinger.

Claim 30 recites:

> A method comprising:
> initiating configuration of a configurable system on chip (CsoC) using an on-chip central processing unit (CPU);
> configuring a memory cell in the CSL using a first device of a group of devices, the group of devices comprising the CPU, a direct memory access (DMA) controller, and an external control device;
> reading a memory cell in the CSL using a second device selected from the group of devices; and
> selecting a signal in the CSoC to determine if the system bus is used for configuration or general interconnect of the CSoC.

(Claim 30). As noted above, Gittinger does not teach or suggest configuring a memory cell in a configurable system logic using a device selected from a group of devices. Furthermore, Gittinger does not teach or suggest selecting a signal to determine if the system bus is being used for configuration or general interconnect. Therefore, claim 30, and claims 31 and 32 which depend on it, are not anticipated by or obvious over Gittinger.

Applicants respectfully submit that Gilson and Gittinger cannot be logically combined. There is no motivation within the references themselves for such a combination. Furthermore, even in combination, the references do not teach or suggest controlling a system bus for configuration using one of a group of devices, as recited in claims 1, 21, and 30. Therefore, claims 1 and 14-32 are not obvious over or anticipated by Gilson and Gittinger.

Applicants respectfully submit that in view of the amendments and discussion set forth herein, the applicable rejections have been overcome. Accordingly the present and amended claims should be found to be in condition for allowance.

If the Examiner finds any remaining impediment to the prompt allowance of these claims that could be clarified with a telephone conference, the Examiner is respectfully requested to contact Judith A. Szepesi at (408) 720-8300.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due and not covered by any check submitted.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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Judith A. Szepesi
Reg. No, 39,393

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, CA 90025
(408) 720-8300

VERSION WITH MARKINGS TO SHOW CHANGES

IN THE CLAIMS

1. (Twice Amended) A method of using a system bus on a configurable system on a chip (CSoC), the CSoC including configurable system logic (CSL), the method comprising:

controlling [determining if] the system bus [is controlled] for configuration [by] using a first device, the first device comprising a selectable one of [selected from a group consisting of] an on-chip central processing unit (CPU), a direct memory access (DMA) controller, and an external control device;

configuring a memory cell in the CSL using the system bus; and

reading the memory cell in the CSL using the system bus.

15. (Once Amended) The method of claim 14 wherein reading a memory cell in the CSL using the system bus is performed by a second device selected from the group consisting of [on-chip-central processing unit (CPU)] the CPU, the direct memory access (DMA) controller, and the external control device.

16. (Once Amended) The method of claim 15 further comprising:

mapping a random access memory (RAM) cell in the CSoC [in to] into the addressable memory space of the system bus.

18. (Once Amended) The method of claim 17 wherein reading the RAM cell using the system bus is performed by a third device selected from the group consisting of [on-chip-central processing unit (CPU)] the CPU, the direct memory access (DMA) controller, and the external control device.